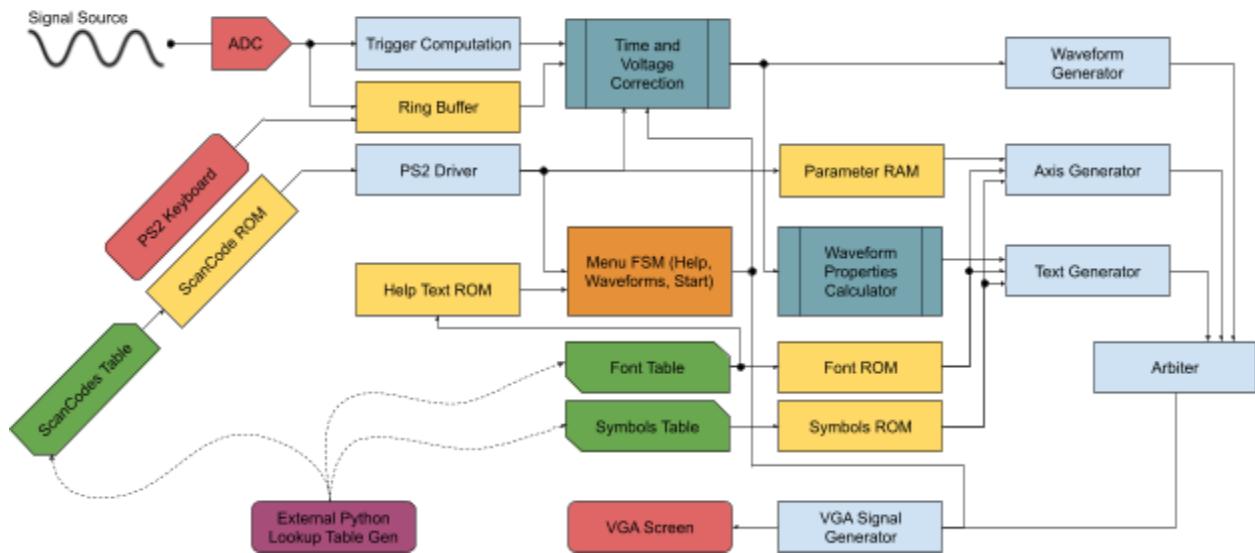


Digital Oscilloscope ECE 241 Milestone #1

Rahil Harit-Singh and Ayan Ali

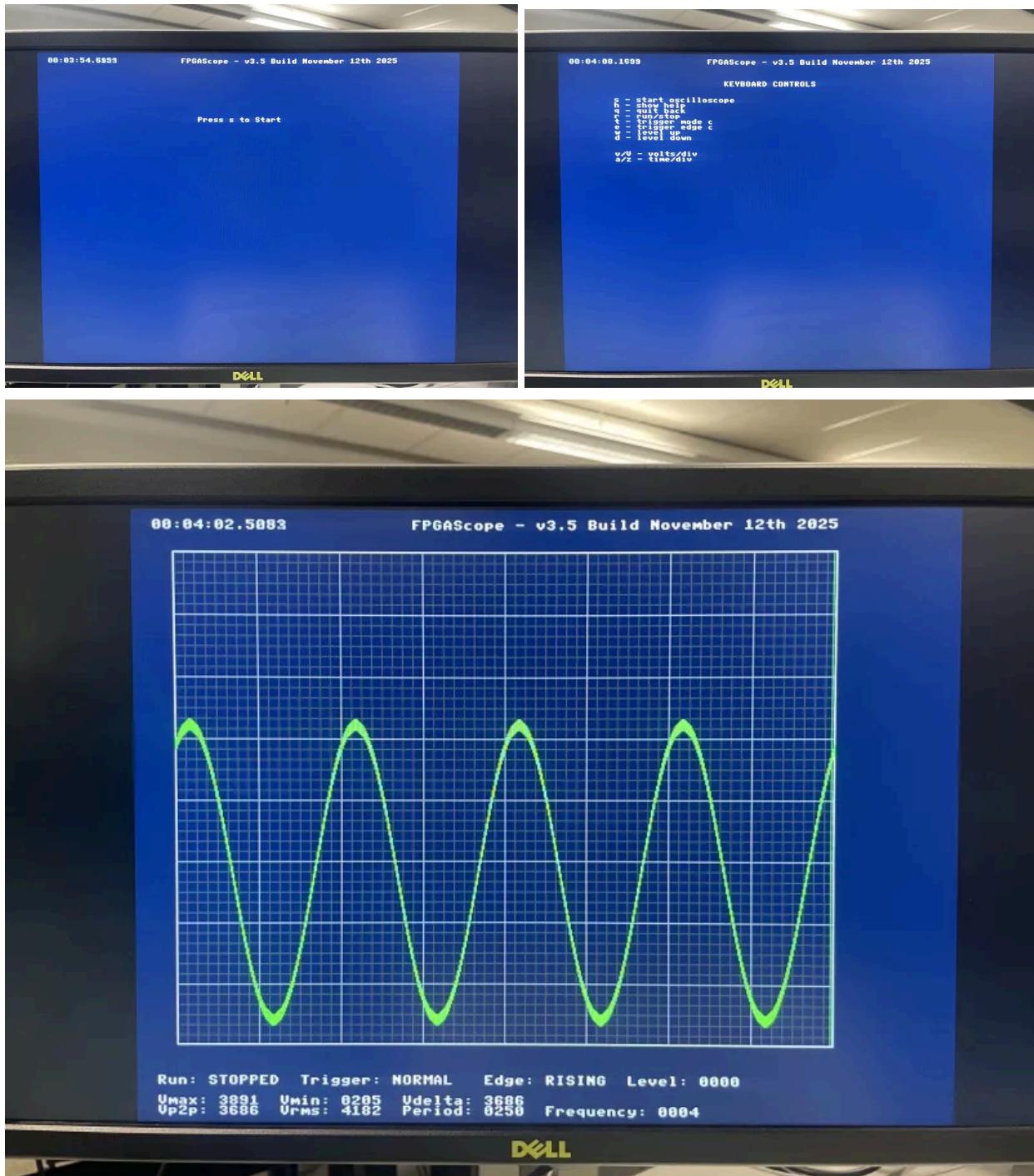
Summary

This week involved the process of setting up the entire pipeline of the project, i.e. writing a VGA driver, PS2 driver, getting a waveform to display on the screen, getting rough calculations of waveform properties to display, and implementing the character display pipeline. This groundwork has set the infrastructure we will use to further develop the features of the FPGAScope, chief of which is getting the ADC to take an analog and place it into the ringbuffer.



Most of the items above have been completed in some capacity save for the trigger computation and time and voltage correction.

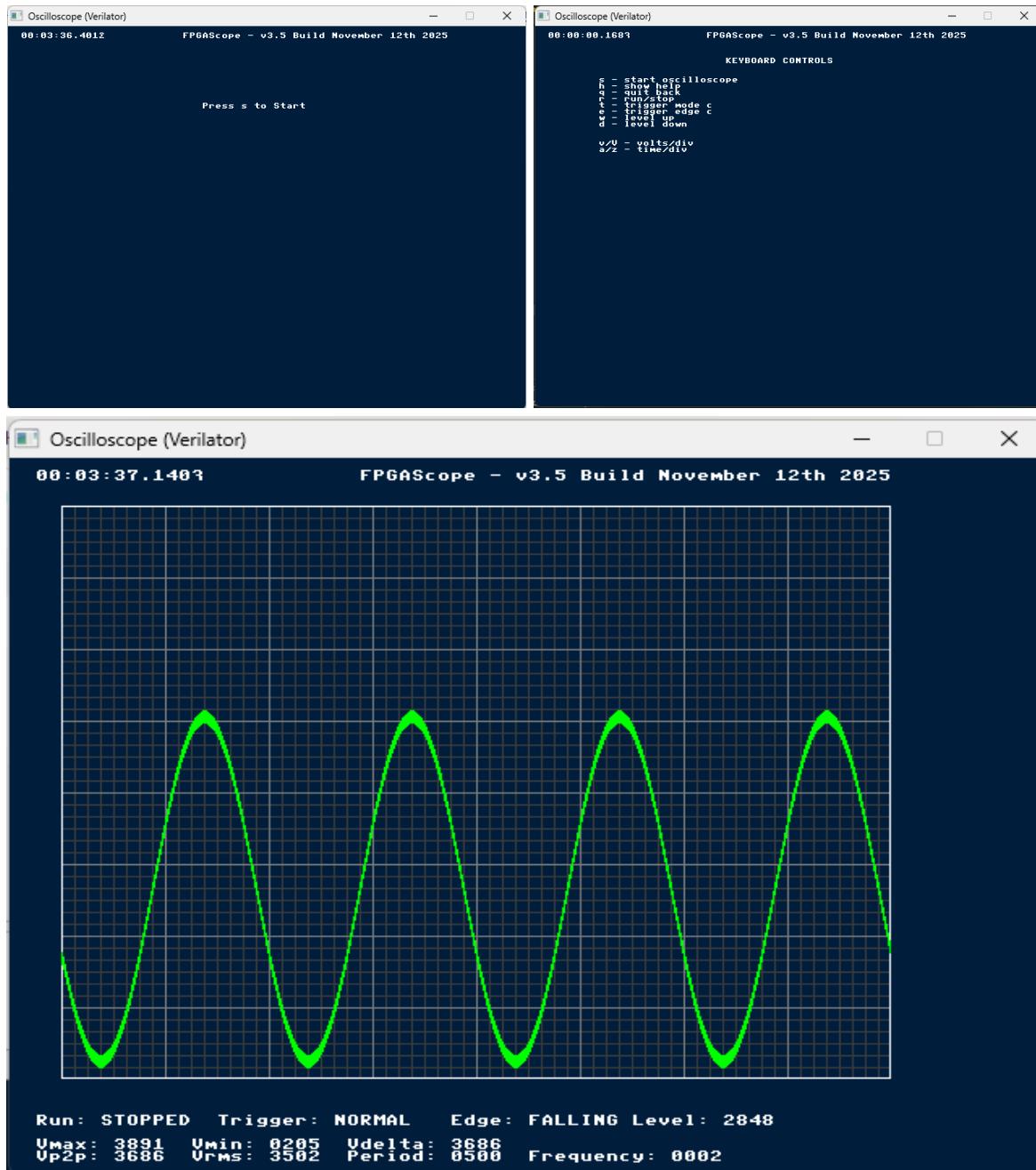
Photos of Progress



Testbenches

DESim is exceptionally slow at rendering windows, not very useful for quickly debugging UI components and for quickly checking if changes to the waveformGenerator module or ps2Driver module are mirrored correctly.

It was very useful as we could not always come into the lab, wrote our modules asynchronously the majority of times, etc. (and stayed up late writing it, not very convenient to come into the lab at 2AM!). Below is what the Verilator has produced, this is the most recent build.



New Ideas Developed

If there is time before the final project the following ideas might be interesting:

1. There is an issue where if a wave is too steep it will have gaps, the temporary way to fix this is make the line thicker, this reduces accuracy. Interpolation using $\sin(x)/x$.
2. Adding a second channel is quite straightforward as it is multiplying most modules x2 and handling the interconnections. We have used a small amount of resources, so this is feasible to do so. Perhaps even 6-channel is feasible given the 6-pin ADC header.

Work Assignments

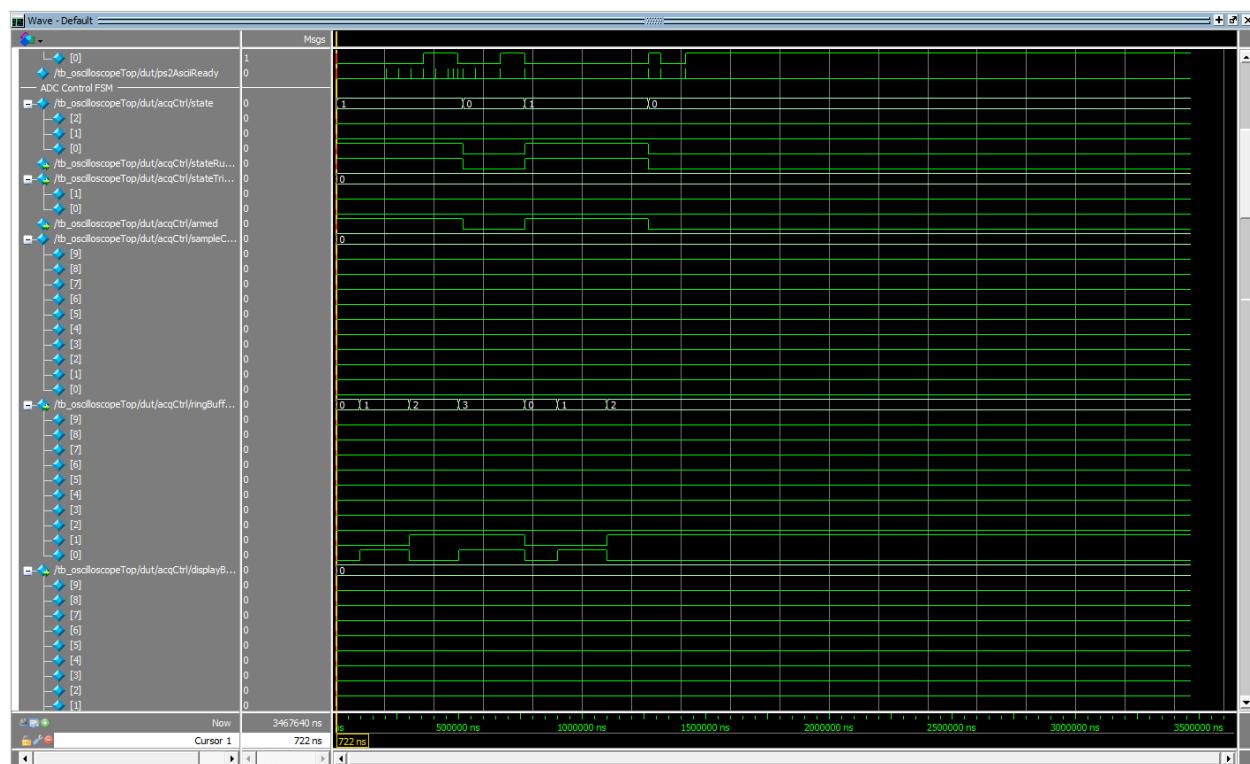
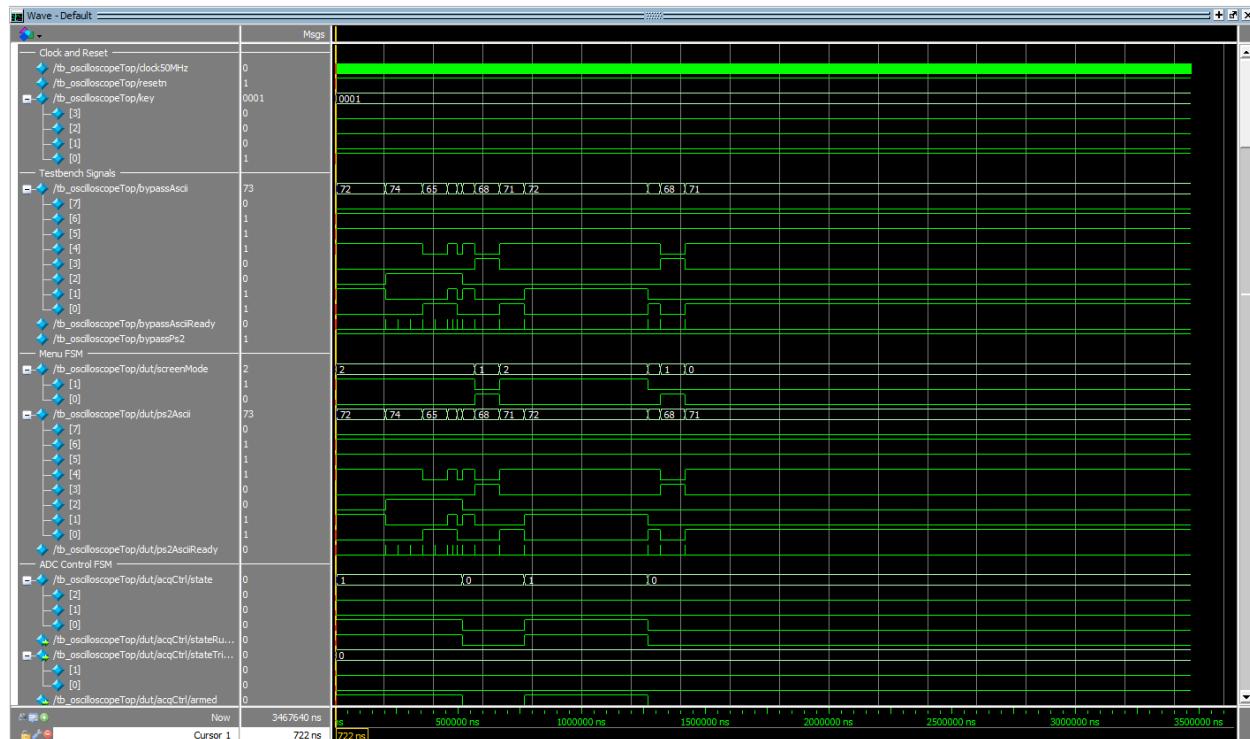
We had aimed to get the below work done in time for the halfway point between Milestone #1 and Milestone #2, hence some parts of the table below are in-progress. Given that during the actually writing of the verilog we discovered that we had to change our timeline slightly some work has been pushed to Milestone #2 and some Milestone #2 has been brought forward to Milestone #1.

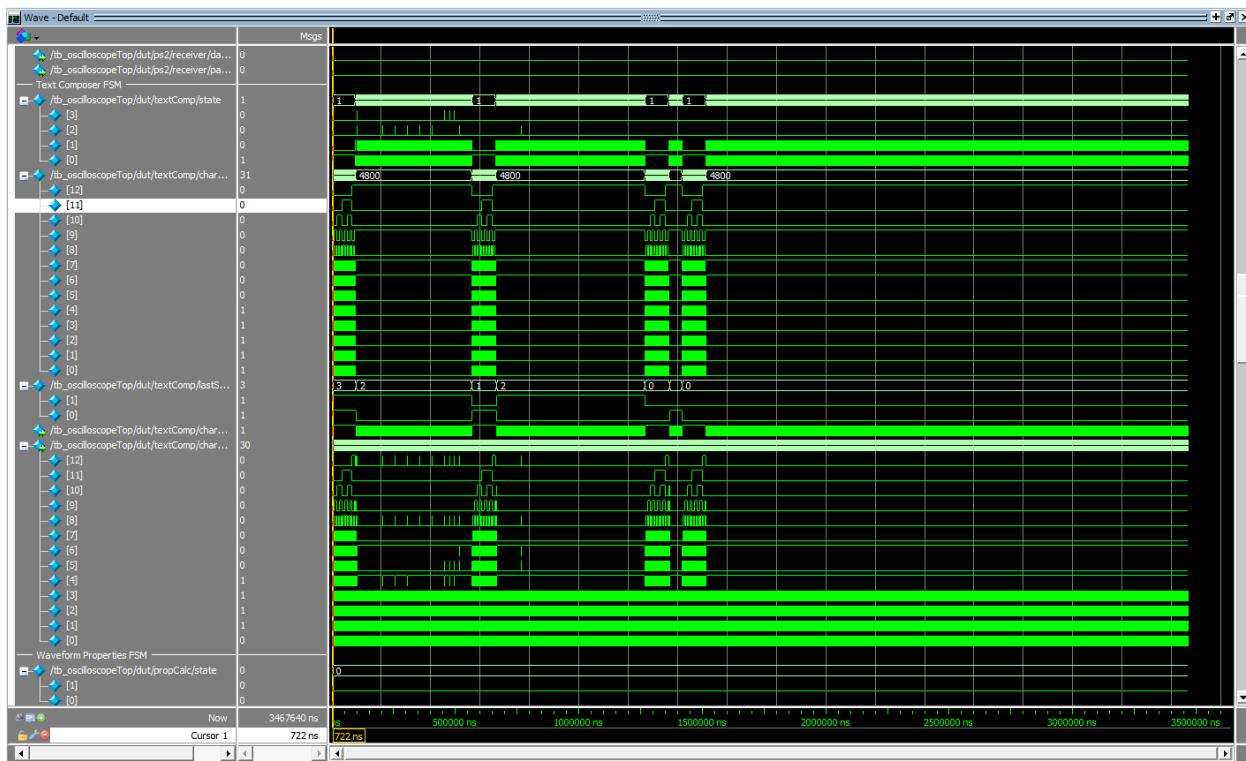
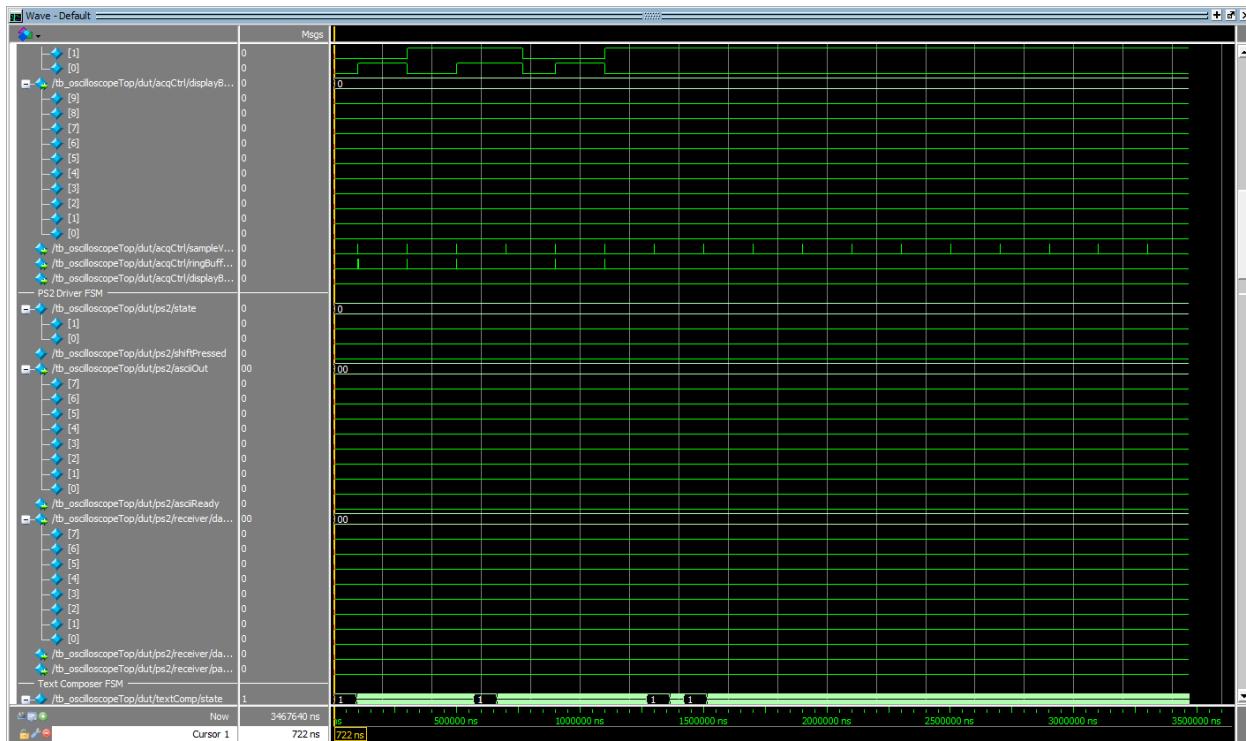
Work labelled DONE is finished. Work labelled IN-PROGRE[SS] is work we aim to finish before the end of the work week.

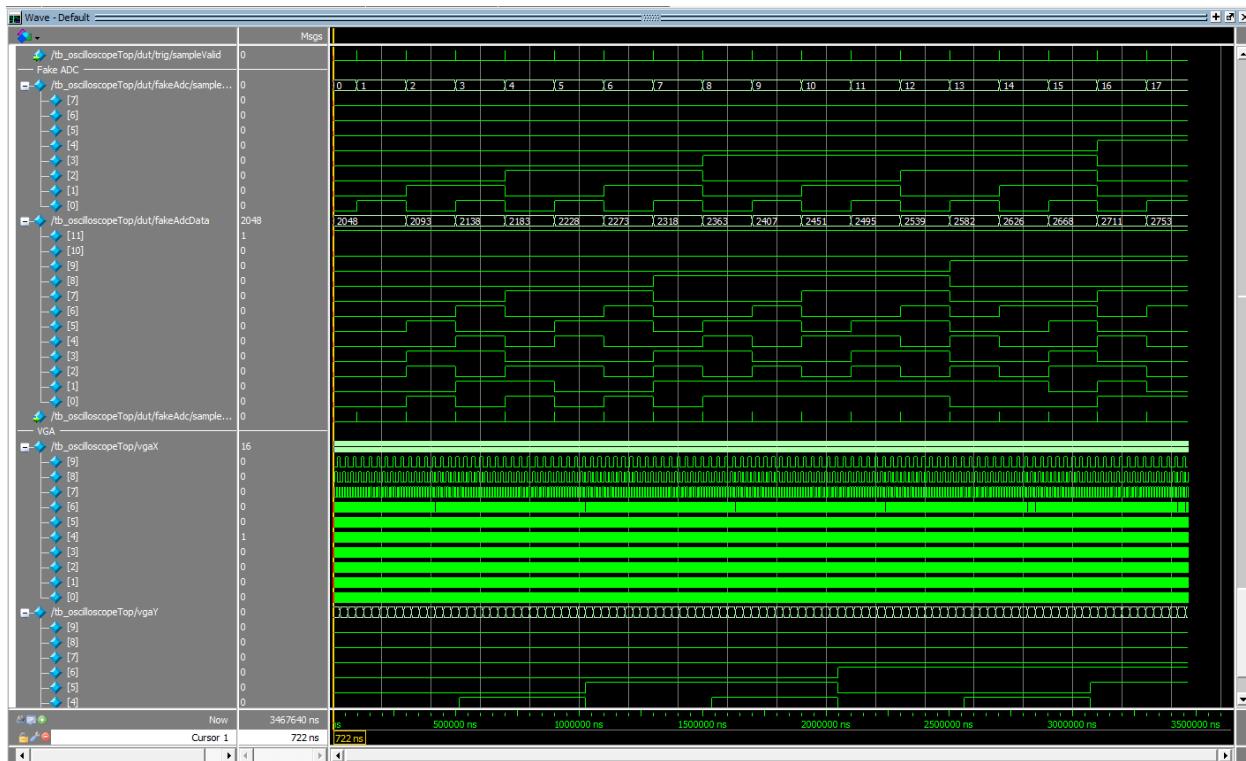
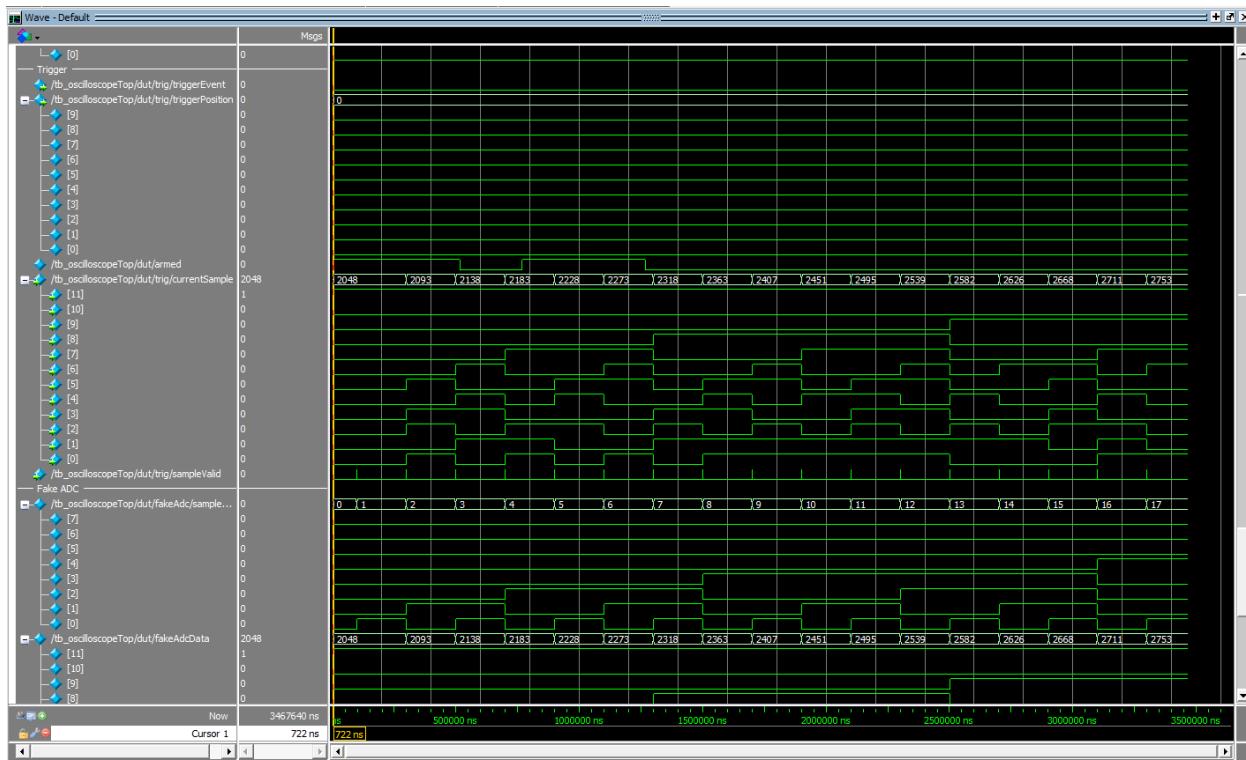
Assignee	Work	Status
Ayan	Verilator Testbench DESim Testbench	DONE DONE
	FakeADC Python Generator and FakeADC.v ScanCodesLUT Python Generator FontLUT Python Generator	DONE DONE DONE
	PS2 (and ScanCodes) and VGA Driver Research State Machines Design	DONE DONE
	ps2Driver.v scancodesROM.v waveformGenerator.v waveformProperties.v menuFSM.v textComposer.v ringBuffer.v	DONE DONE DONE DONE DONE DONE DONE
	oscilloscopeTop.v waveformTrigger.v timeVoltageCorrection.v bridgeAD7928toSPI.v	IN-PROGRE IN-PROGRE IN-PROGRE IN-PROGRE
	Milestone #1 Writeup Draw Cool Logo + Parsing for Display	DONE IN-PROGRE
Rahil	ModelSim Testbenches	DONE

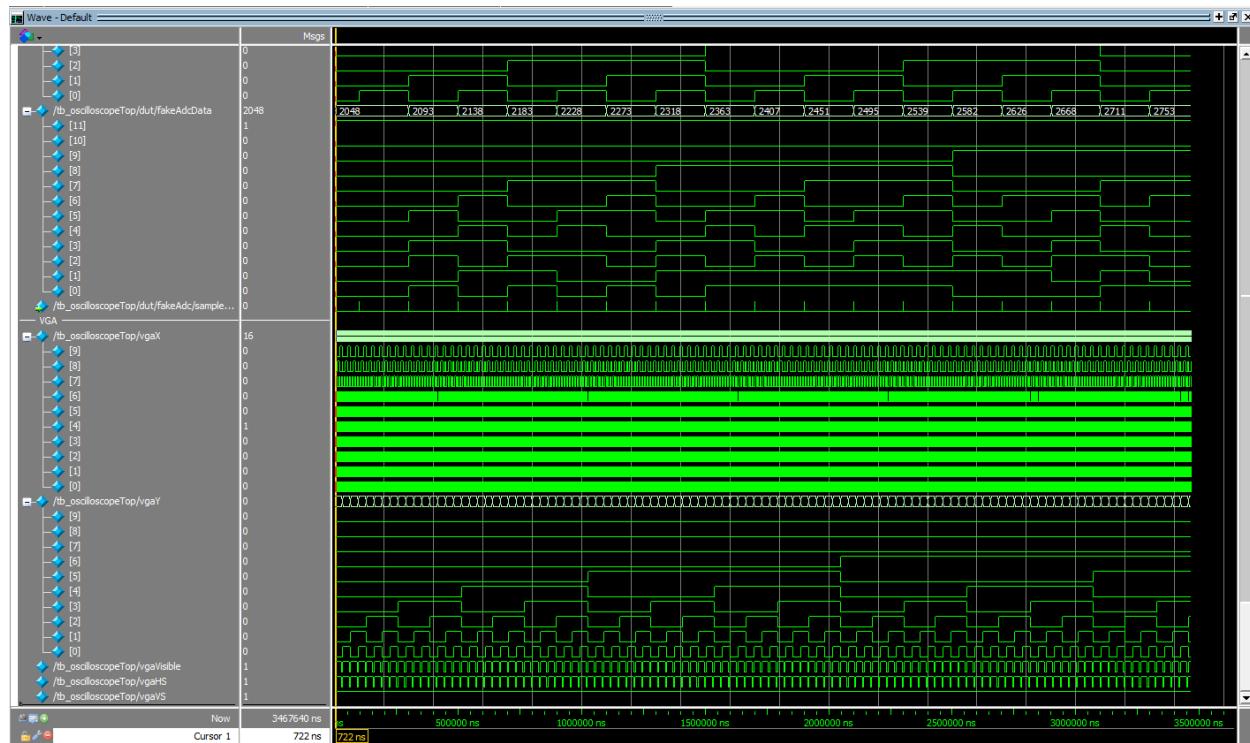
	vgaDriver.v fontROM.v parameterRAM.v characterRAM.v textGenerator.v axisGenerator.v pixelArbiter.v displayBuffer.v clockCounter.v controlADC.v	DONE DONE DONE DONE DONE DONE DONE DONE DONE IN-PROGRE
	Milestone #1 Writeup Draw Cool Logo + Parsing for Display	DONE IN-PROGRE

ModelSim Testing of Statemachines

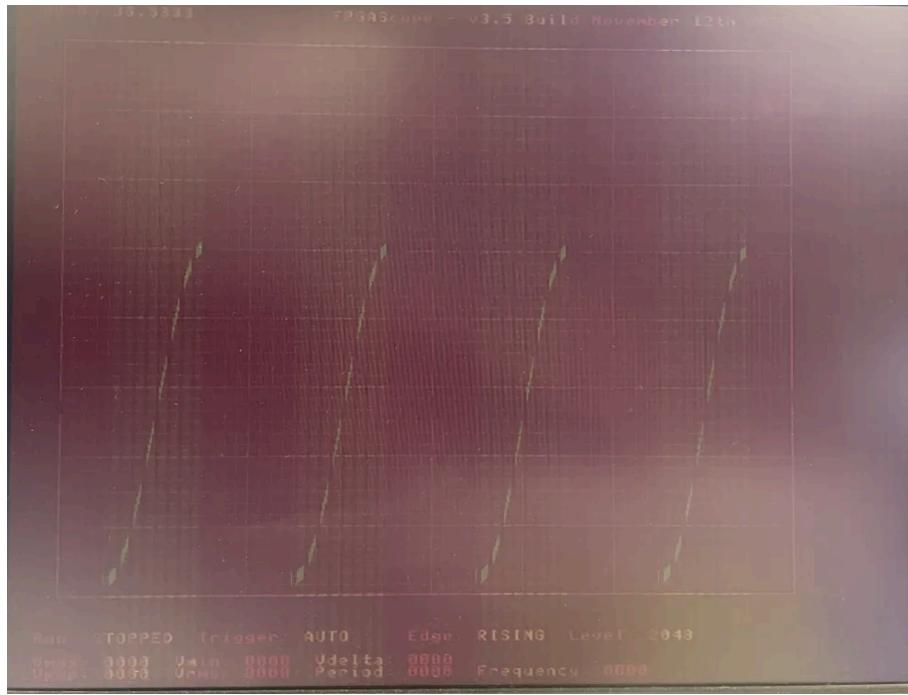




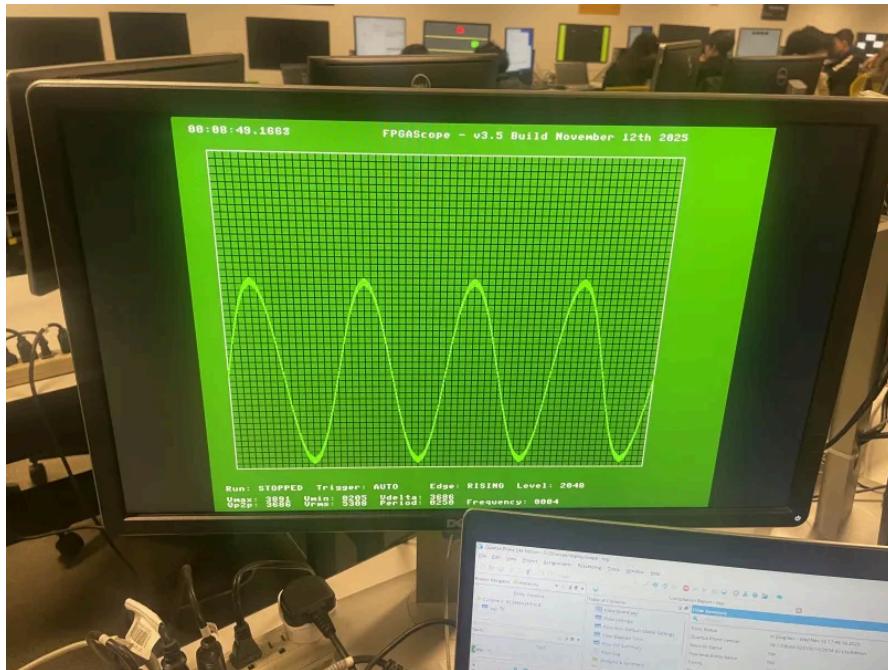




Spooky Bugs



This display bug happened as my code handles only 4-bit color in an effort to reduce displayBuffer.v size. The vga screen expects a 8-bit color for each RGB. This fix was to add extra bits to the end of the color value when passing to VGA.



This display bug happened when the green and blue connection wires were flipped due to a typo.